Background Information

Commented [CJ1]: Helpful to share with students

Transistors work because of the layered sandwiching of two different types of semi-conductors. A basic gate type of transistor works by having a source and drain that cannot have current flow between them unless a gate is "opened". The gate operates by have a voltage applied to it or not having a voltage applied to it. When a voltage is applied to the gate, it allows electrons to flow between the source and drain, resulting in the gate being open. If the voltage is not applied, electrons cannot flow from source to drain, meaning the gate is closed. When running calculations, inputed values are typically controlling this gate, turning a current on or off to perform operations.

As programs became more and more complex, the number of operations that need to be performed have grown exponentially, meaning that the number of transistors needed has also grown exponentially. However, devices have not grown in physical size exponentially, instead, going against the trend and getting smaller. This is because transistors have been getting smaller and smaller. Industry has tried to follow a rule called Moore's Law, which basically states that the number of transistors that will fit in a given area will double every two years. In order to achieve this, manufacturers used a process called Dennard Scaling, which reduced every parameter of transistors by about 30%.

We are going to model this scaling in a lab using legos to build two subsequent generations of transistors from a parent generation. The goal of this lab is to show how a reduction in parameters of 30% leads to a reduction in area of approximately 50% and to also introduce the current dilemma that manufacturers face, which is that it is getting to a point where it is physically impossible to reduce the size of transistors. (Some components of state of the art transistors are measured in angstroms, which is the approximate width of an atom.)

Students should read http://www.nature.com/news/the-chips-are-down-for-moore-s-law-1.19338 as part of the introductory lesson before completing this lab to also get a better understanding of the overall picture of transistors.

Materials

Commented [CJ2]: For Teachers

Assorted Legos

Lego base plates ~10”x10”

Set Up

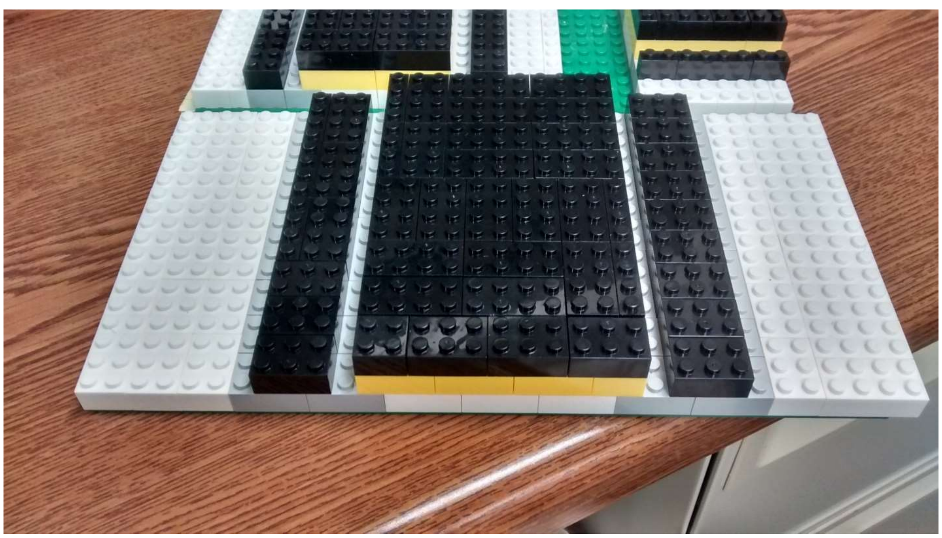
Build a large model transistor on one of the baseplates. I suggest laying out a rectangle that is 33 studs long and 18 studs wide. Alternate colors (I used white and grey) along the length of this base rectangle 6 studs white/6 grey/9 white/6 grey/6 white. The two grey sections represent the source and drain areas of the transistor. This is the area that is made up of silicon (n- and p- type).

On top of the grey areas, lay down a strip of black that is 3 studs wide. There should be one stud of grey showing towards the outside of the rectangle, and two studs of grey showing towards the inside of the rectangle. Do this over both grey areas. These two strips of black represent the source and drain connections to the transistor.

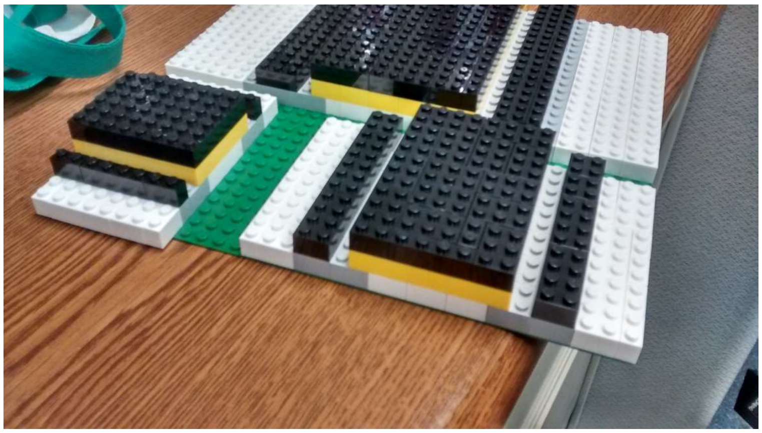
Between the two strips of black that you laid down, lay down a new color (I used yellow), leaving one stud of spacing between the yellow bricks and the black bricks. The studs showing between the yellow and black bricks should be grey from the base rectangle. This yellow layer represents an oxide barrier between the gate that we will make next, and the silicon.

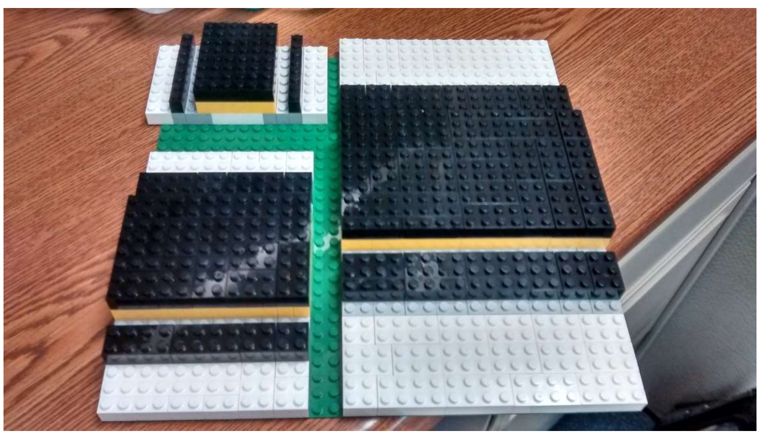
Finally, on top of the yellow bricks, lay down a layer of black bricks that completely covers the yellow. This last layer of black bricks represents the gate of the transistor and controls whether or not electrons will be able to flow from the source to the drain (The two grey areas).

Here is a picture of one that I completed. You may choose to modify these dimensions if you wish. I chose them because most will scale perfectly, but some will present a challenge to students that can be discussed.



I have also included a picture of how I created the 2nd and 3rd generation, or scaled transistors and a picture of all three at the same time.

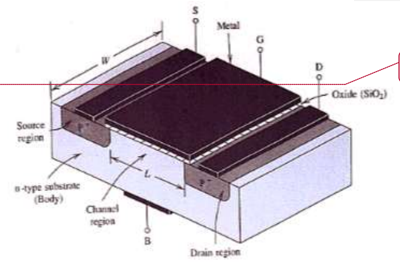




Finally, to culminate this project, you may choose to have students graph the trends in how many transistors are fitting on the baseplate and create a model for how many transistors there will be. You can also then make predictions based on the model. For advanced students, you may even choose to have a discussion about using semi-log graphs to plot the data.

Moore's Law and Transistors

Visualizing the diminishing size of transistors and issues stemming from this



Commented [CJ3]: Start of Lab

1) What is Moore's Law?

Commented [CJ4]: The number of transistors that fit within a given area will double every 2 years.

In order to achieve the desired scaling and stick to Moore's Law, transistors have had their dimensions scaled down by about 30% with each successive generation. For example, Intel transistor sizes have gone from 65 nm in 2006, to 45 nm in 2008, to 32 nm in 2010 to 22 nm in 2012.

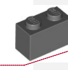
2) Find the percentage that each successive generation decreased from its preceeding generation. (Find the % that each successive generation is compared to its preceeding generation. Then, what percentage was lost?)

   a. 2008:_______
   b. 2010:_______
   c. 2012:_______

Commented [CJ5]: A) 45/65 = .6923; 1-.6923 = .3077 = 30.77%
B) 32/45 = .7111; 1-.7111 = .2889 = 28.89%
C) 22/32 = .6875; 1-.6875 = .3125 = 31.25%

Now, get a lego baseplate. This is going to be your “processor” and we are going to look at how many transistors we can fit on it. To start, lets figure out how much area we have to work with.

3) Figure out the area of your empty “processor” baseplate in terms of studs. (The standard little lego piece has two studs)



Commented [CJ6]: The plates that I used are 32x32 = 1024 studs

The first generation transistor that we are starting with was made by the teacher. Go to the front of the room and look at this transistor.

4) Find the area and dimensions of each colored portion of the transistor.

Commented [CJ7]: WhiteLeft:6x18 = 108 studs
White Mid: 9x18 = 162 studs
White Right: 6x 18 = 108 studs
Black Left: 3x18 = 54 studs
Black Mid: 11x18 = 198 studs
Black Right: 3x18 = 54 studs
Grey Left: 6 x 18 = 108 studs
Grey Right: 6x 18= 108 studs
Yellow: 11x18 = 198 studs

White Left:	White Middle:	White Right:
Black Left:	Black Middle:	Black Right:
Grey Left:	Grey Right:	Yellow:

5) Calculate the area of the entire transistor in studs (Note, the transistor is slightly larger than the “processor” and its area is not the same as the sum of all of its parts since some are stacked).

Commented [CJ8]: 33 X 18 = 594 studs

6) Approximately how many transistors would fit on your “processor” based on area alone?

Commented [CJ9]: 1024/594 = 1.724; so approximately 2 transistors.
Students could argue that you don’t have room to fit 2, so 1 would also be acceptable.

Now, we are going to build the 2nd generation transistor by decreasing the dimensions of the original transistor by 1/3, or 33%.

7) Build this second generation transistor on your baseplate/"processor"(You may not have enough of the same color, so you may need to change your colors, like change white to red, or black to green.) Not everything may scale perfectly, so try to create the best representation of the original as possible. When you finish building it, call your instructor over to discuss your design and any decisions you made constructing it. You must have your design signed off by the teacher before moving on.

Design meets requirements:___________________________

8) Find the area and dimensions of each colored portion of the 2nd generation transistor.

White Left:	White Middle:	White Right:
Black Left:	Black Middle:	Black Right:
Grey Left:	Grey Right:	Yellow:

9) Were any of the dimensions hard to scale down? If so, what did you decide to do to scale them? In not, do you forsee any problems in the future?

10) What is the area in studs of the entire 2nd generation transistor?

11) Approximately how many of these transistors would fit on our "processor" based on area alone?

Commented [CJ10]: If students struggle here, it is helpful to give to design parameters:
1)The middle portion must overlap the two grey areas representing the source and drain.
2)The three black portions cannot be in direct contact, as then current would flow freely between them.

Commented [CJ11]: These numbers are not set in stone, as students may rationalize slightly different designs, but dimensions should be close to this.
WhiteLeft:4x12 = 48 studs
White Mid: 6x12 = 72 studs
White Right: 4x 12 = 48 studs
Black Left: 2x12 = 24 studs
Black Mid: 8x12 = 96 studs (or 7x12=84 studs)
Black Right: 2x12 = 24 studs
Grey Left: 4 x 12 = 48 studs
Grey Right: 4 x 12= 48 studs
Yellow: 8x12 = 96 studs (or 7x12=84 studs)

Commented [CJ12]: Students should have had a slight problem scaling the middle black/yellow portion. They may have chosen to make the portions 7 or 8 studs wide. 7 more closely follows the scaling, whereas 8 more closely follows the design.
Students may also have had issues with the gaps between the black portions since you cannot scale a gap of 1 stud.

Commented [CJ13]: 12x22 = 264 studs

Commented [CJ14]: 1024/264=3.879; so approximately 4, although students could argue 3.

Now, we are going to make a 3rd generation transistor by scaling down our 2nd generation transistor. Once again, decrease each dimension by 1/3, or 33%.

12) Build the new transistor on your baseplate/"processor".
    Teacher Approval of design:___________________
13) Find the area and dimensions of each colored portion of the 3rd generation transistor.

White Left:	White Middle:	White Right:
Black Left:	Black Middle:	Black Right:
Grey Left:	Grey Right:	Yellow:

14) Many decisions were made as you scaled down your transistors in this lab. Justify your 3rd generation design and the choices your team made getting to this design. Be sure to reference specific choices that were made and why these choices led to the design your group felt was best.

15) What is the area in studs of the 3rd generation transistor?

16) Approximately how many of these transistors would fit on your "processor"?

Commented [CJ15]: Dimensions may be off by 1 on many of these based student decisions. Be sure to discuss decisions with the class/groups

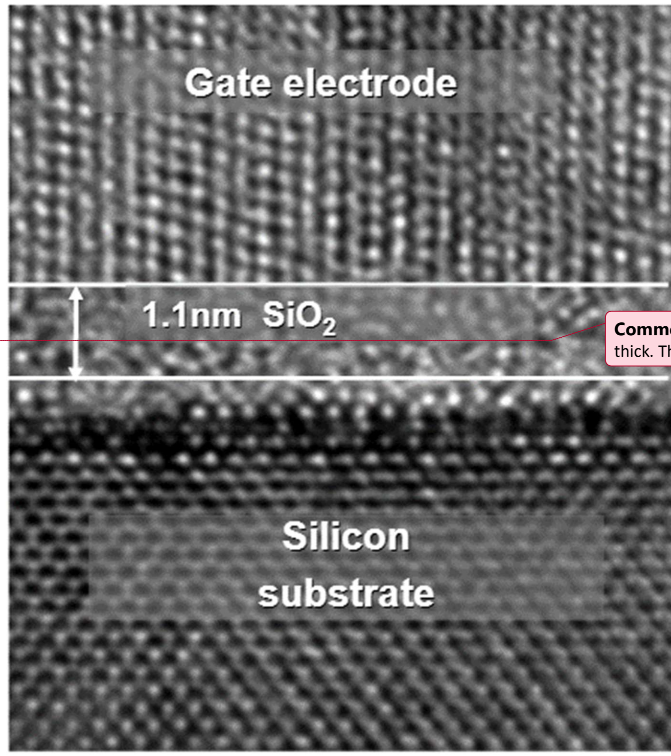
WhiteLeft:3x8 = 24 studs
White Mid: 4x8 = 32 studs
White Right: 3x 8 = 24 studs
Black Left: 1x8 = 8 studs
Black Mid: 6x8 = 48 studs
Black Right: 1x8 = 8 studs
Grey Left: 3 x 8 = 24 studs
Grey Right: 3 x 8= 24 studs
Yellow: 6x8 = 48 studs

Commented [CJ16]: Students should rationalize the rounding decisions that they made a justify the overall design of their final transistor compared to the original design.

Commented [CJ17]: 8x16 = 128 studs
(Base should scale to this, as it took no rounding to get here.)

Commented [CJ18]: 1024/128 = 8 transistors

17) To the right is a picture of part of a transistor on the INTEL 65 nm Pathfinder transistor. The 1.1nm SiO_2 section is what the yellow represented on our model. Each little bump is one atom. About how many bumps wide is the SiO_2 in the picture?



Commented [CJ19]: The Silicon Oxide is about 5 atoms thick. This is an actual picture of an INTEL Transistor.

18) Given your experience with the models you made and information shown in the given picture, what fundamental issue will be faced if industry continues to scale down transistors at the same rate?

Commented [CJ20]: Aside from the obvious problems with cost to produce such precise hardware, if scaling were to try and move forward, you will eventually get to transistor parts that are only 1 or 2 atoms thick, at which point it is impossible to scale any further.

19) Now, look back at your answers to #6, 11, and 16. Fill them in on the table below, and then fill in your predictions for theoretical 4th generation and beyond transistors that would follow the same scaling pattern. (Hint: Would this scale linearly, exponentially, quadratically…)

Commented [CJ21]: The first three blanks would be filled in from previous answers, and should be close to 2, 4, 8. Hopefully, students will come up with a similar pattern for their prediction and have numbers close to doubling each time, which should leave you with about 1000 transistors for the 10th generation.

Transistor Generation	Number of Transistors on Board
1st	
2nd	
3rd	
4th	
5th	
6th	
7th	
8th	
9th	
10th	

20) Describe how you made your predictions for the 4th through 10th generation transistors. Be sure to include any patterns that you used as part of your answer and why you chose that pattern.

Commented [CJ22]: Students should notice numbers come close to doubling and then use that doubling to make their predictions for the future generations.

21) Now, graph the transistor generations vs. the number of transistors on the grid below. Be sure to title, label, and scale your graph.

22) Now, look back at your answers to #5, 10, and 15. Fill them in on the table below, and then fill in your predictions for theoretical 4^{th} generation and beyond transistors that would follow the same scaling pattern.

Transistor Generation	Area of Transistor in studs
1^{st}	
2^{nd}	
3^{rd}	
4^{th}	
5^{th}	
6^{th}	
7^{th}	
8^{th}	
9^{th}	
10^{th}	

Commented [CJ23]: The first three blanks would be filled in from previous answers, and should be 594, 264, and 128. Hopefully, students will come up with a similar pattern for their prediction and have numbers close to halving each time, (actually a bit less than half, as scaling by 1/3 would reduce size by 56% if done exactly) which should leave you with about 1 to 0.5 studs for the 10^{th} generation.

23) Describe how you made your predictions for the 4^{th} through 10^{th} generation transistors. Be sure to include any patterns that you used as part of your answer and why you chose that pattern.

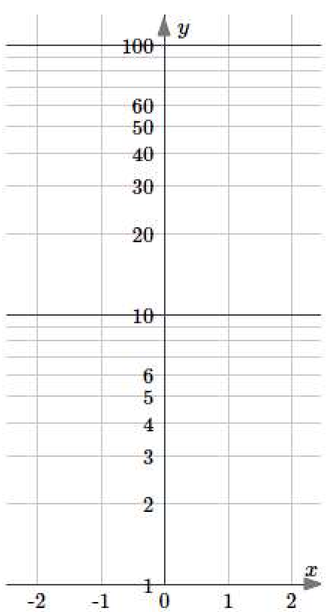
Commented [CJ24]: Students should notice numbers come close to halving and then use that halving to make their predictions for the future generations.

24) Now, graph the transistor generations vs. the area of the transistor on the grid below. Be sure to title, label, and scale your graph.

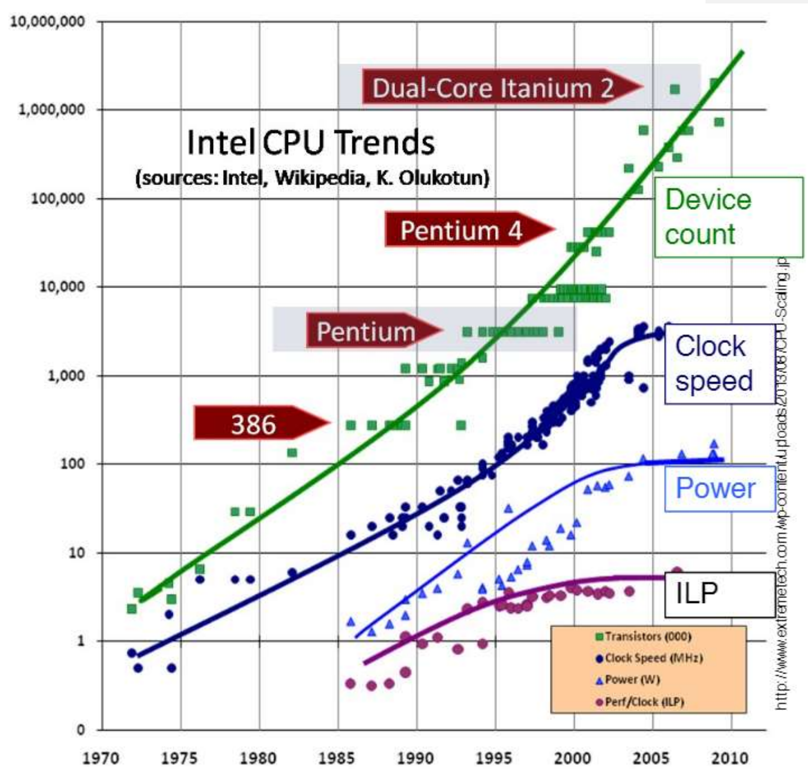
25) You should notice an exponential relationship in each of your graphs above. Oftentimes, this is difficult to graph. What problems did you have trying to graph your data above?

Commented [CJ25]: Scale is often a difficult choice to make with exponentials since the difference between each data point either grows/shrinks at a greater rate as you progress through your data.

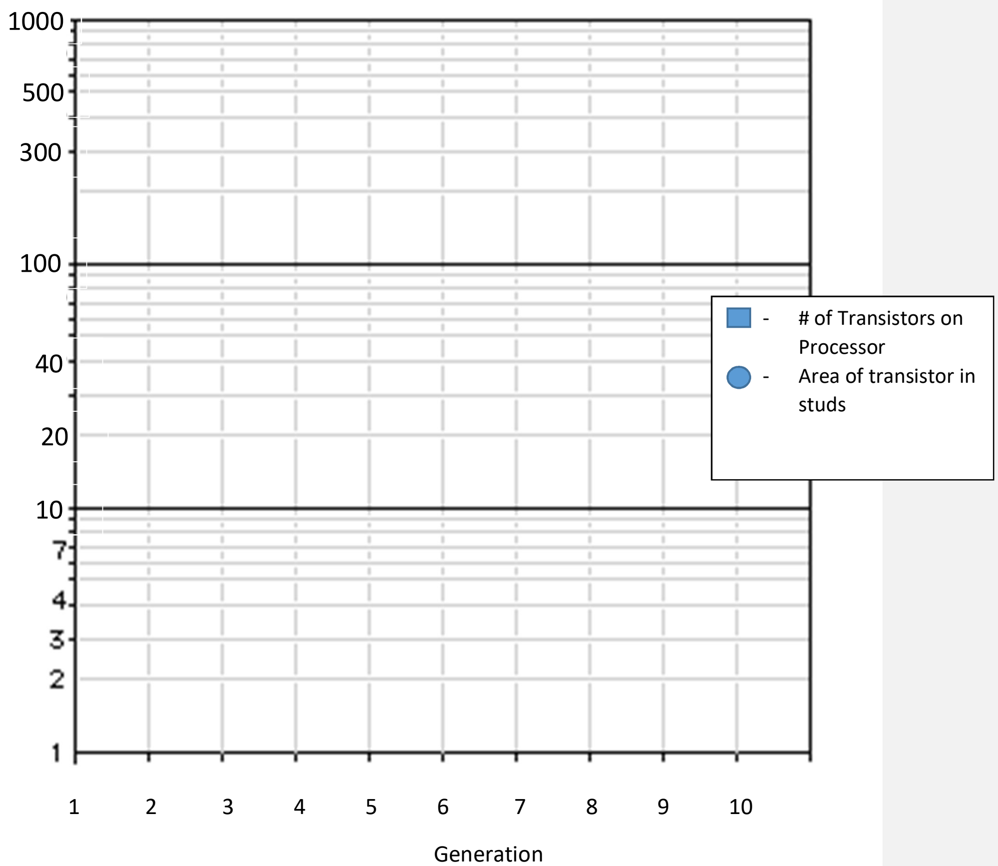
One way to deal with scaling is to use a type of graph called a semi-log graph. This uses one scale that increases exponentially on a logarithmic scale instead of linearly. An example of the scaling is shown below next to a semi-log graph showing characteristics of processors throughout the years. Carefully look at the pattern on the y-axis.



Semilogarithmic axes.



26) Now, try graphing your data on the given Semi-Log graph below. Graph both sets of data.



27) How does this graph look different from the first graphs that you made? Be specific about the shape of the graph.